STP6301D

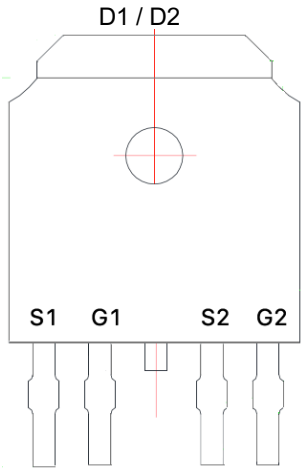
N&P Pair Enhancement Mode MOSFET

23.0A / -18.0A

DESCRIPTION

The STP6301D is the N & P-Channel enhancement mode power field effect transistor using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. This device is particularly suited for low voltage application such as power management, where high-side switching, low in-line power loss and resistance to transient are needed.

PIN CONFIGURATION
TO252-4L



FEATURE

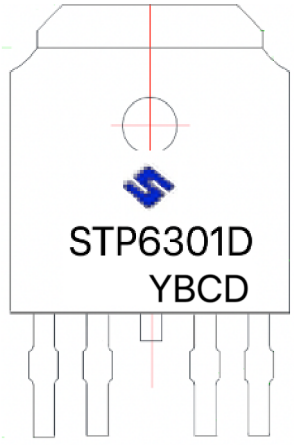
N-Channel

- 60V/8.0A, $R_{DS(ON)}$ = 28mR @V_{GS} = 10V
- 60V/5.0A, $R_{DS(ON)}$ = 37mΩ @V_{GS} = 4.5V

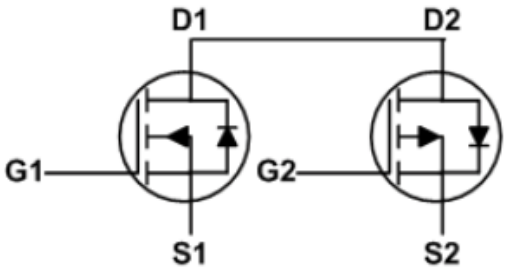
P-Channel

- -60V/-5.0A, $R_{DS(ON)}$ = 46mΩ @V_{GS} = -10V
- -60V/-3.0A, $R_{DS(ON)}$= 65mΩ @V_{GS} = - 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO252-4L package

PART MARKING



Y ： Year code
B ： Date code
C ： Wafer Code
D ： Package Code



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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical N	Typical P	Unit
Drain-Source Voltage		V_{DSS}	60	-60	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Continuous Drain Current	T_A=25℃ T_A=70℃	I_D	23.0 15.0	-18.0 -11.0	A
Pulsed Drain Current		I_{DM}	46	-36	A
Continuous Source Current (Diode Conduction)		I_S	59	-50	A
Power Dissipation	T_A=25℃	P_D	34.7	34.7	W
Operation Junction Temperature		T_J	150		℃
Storgae Temperature Range		T_{STG}	-55/150		℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	85	85	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=10mA V_{GS}=0V,I_D=-10mA	N P	60 -60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=VGS,I_D=250 uA V_{DS}=VGS,I_D=-250uA	N P	1.0 -1.0		2.5 -2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V V_{DS}=0V,V_{GS}=±20V	N P			±100 ±100	nA
Zero Gate Voltage Drain Current	I_{DSS} T_J=25℃	V_{DS}=48V,V_{GS}=0V V_{DS}=-48V,V_{GS}=0V	N P			1 -1	uA
	T_J=55℃	V_{DS}=32V,V_{GS}=0V V_{DS}=-32V,V_{GS}=0V	N P			5 -5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=8.0A V_{GS}=-10V,I_D=-5.0A	N P		0.028 0.046	0.037 0.060	Ω
		V_{GS}=4.5V, I_D=5.0A V_{GS}=-4.5V,I_D=-3.0 A	N P		0.037 0.065	0.045 0.090	
Forward Tran Conductance	gfs	V_{DS}=5V,I_D=8.0A V_{DS}=-5V,I_D=-5.0A	N P		21 15		S
Diode Forward Voltage	V_{SD}	I_S=1.0A,V_{GS}=0V I_S=-1.0A,V_{GS}=0V	N P			1.2 -1.2	V
Dynamic							
Total Gate Charge	Q_g	**N-Channel** V_{DS}=48V,V_{GS}=4.5V I_D≡8.0A **P-Channel** V_{DS}=-48V,V_{GS}=-4.5V I_D≡-5.0A	N P		12.6 9.9		nC
Gate-Source Charge	Q_{gs}		N P		3.5 3.1		
Gate-Drain Charge	Q_{gd}		N P		6.3 3.0		
Turn-On Time	$t_{d(on)}$ tr	**N-Channel** V_{DS}=30V,R_G=3.3Ω I_D=8A,V_{GS}=10V **P-Channel** V_{DS}=-20V,R_G=3.3Ω I_D=-1A,R_{GS}=-10V	N P		8 9.7		nS
			N P		14.2 18		
Turn-Off Time	$t_{d(off)}$ tf		N P		24.6 45.8		
			N P		4.6 45.8		

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TYPICAL CHARACTERICTICS (N MOS)

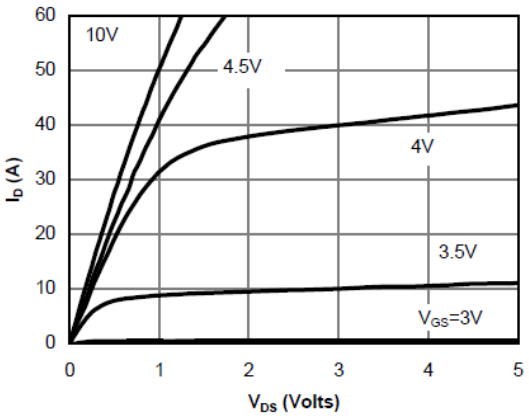

Fig 1: On-Region Characteristics (Note E)

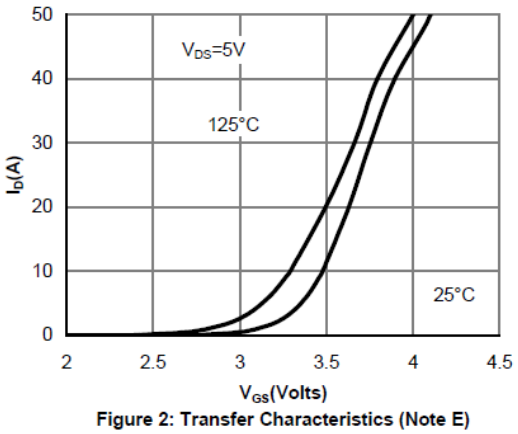

Figure 2: Transfer Characteristics (Note E)

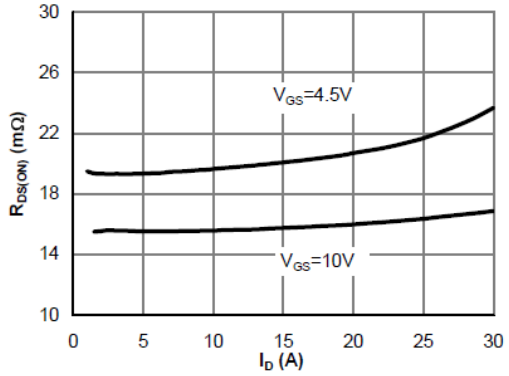

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

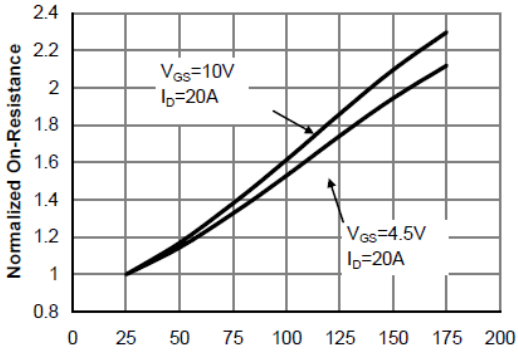

Figure 4: On-Resistance vs. Junction Temperature (Note E)

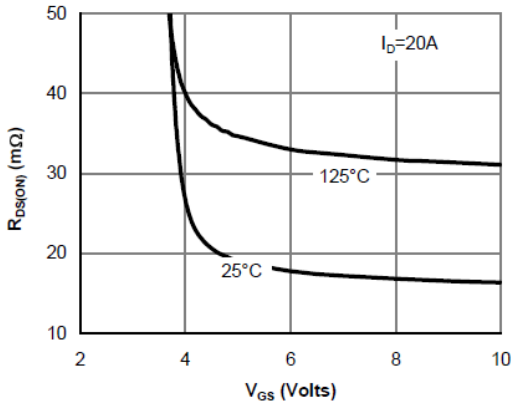

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

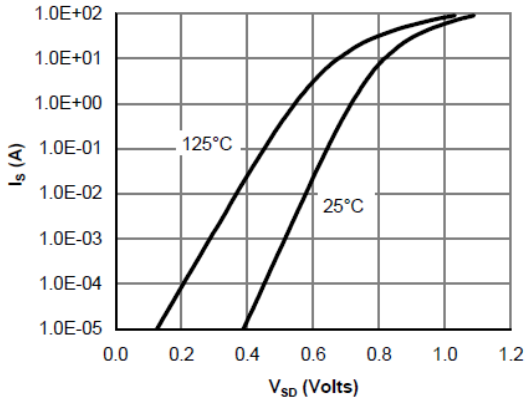

Figure 6: Body-Diode Characteristics (Note E)

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TYPICAL CHARACTERICTICS (N MOS)

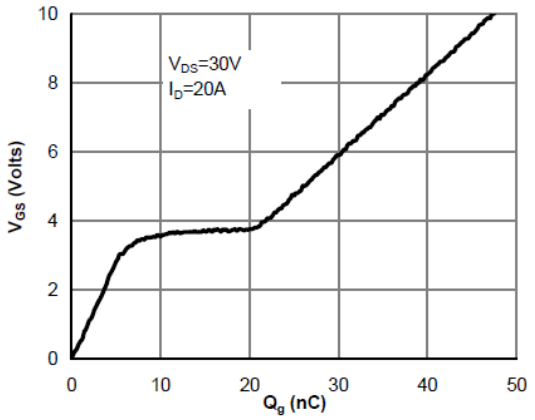


Figure 7: Gate-Charge Characteristics

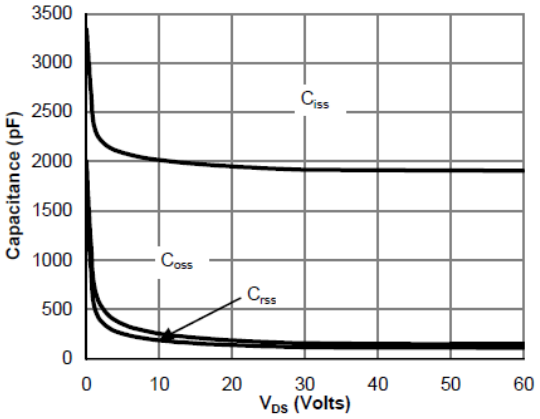


Figure 8: Capacitance Characteristics

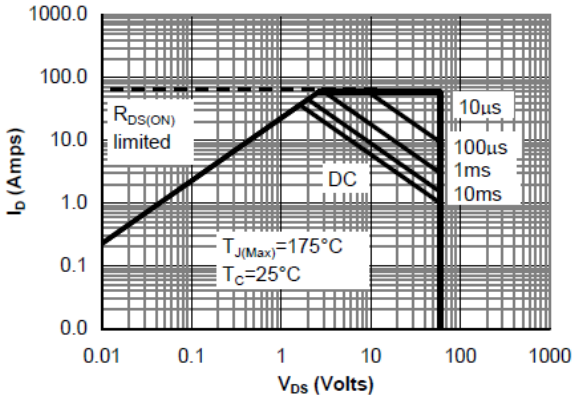


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

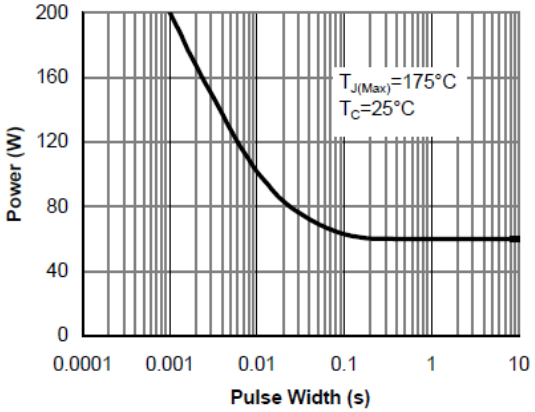


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

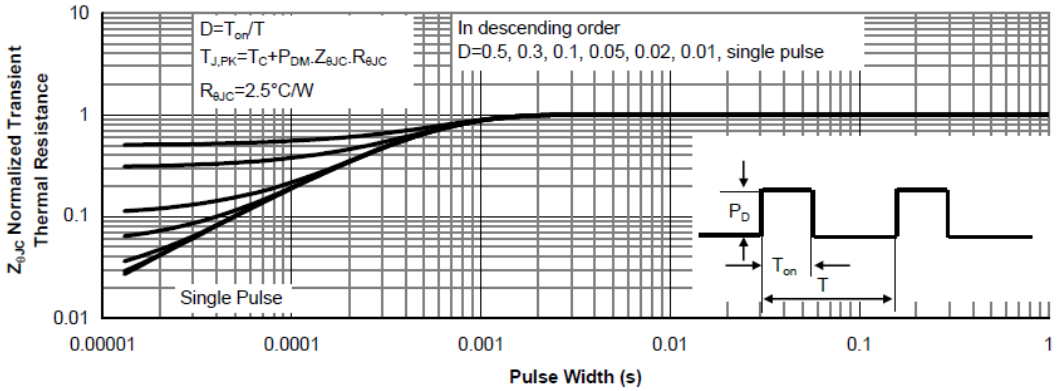
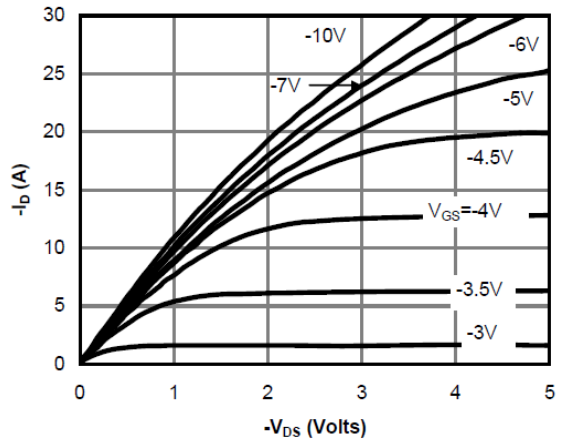


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

YPICAL CHARACTERICTICS (P MOS)



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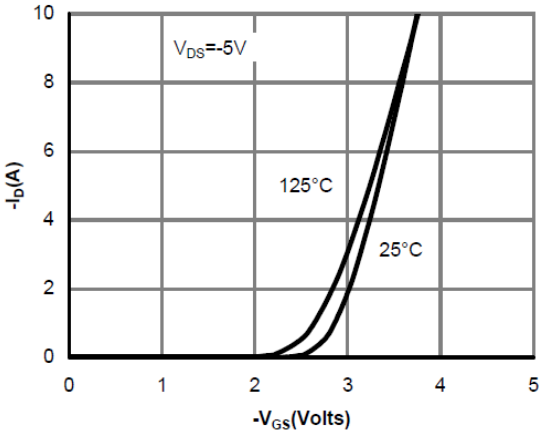


Figure 2: Transfer Characteristics

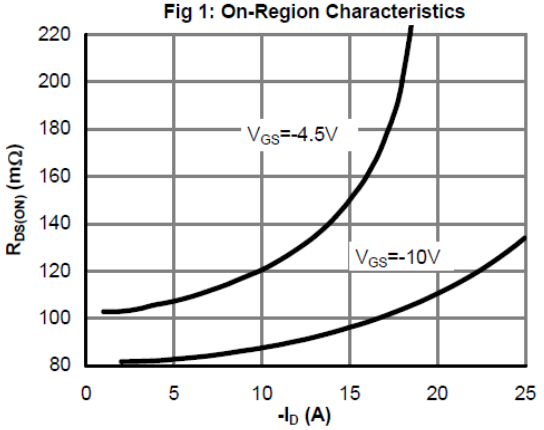


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

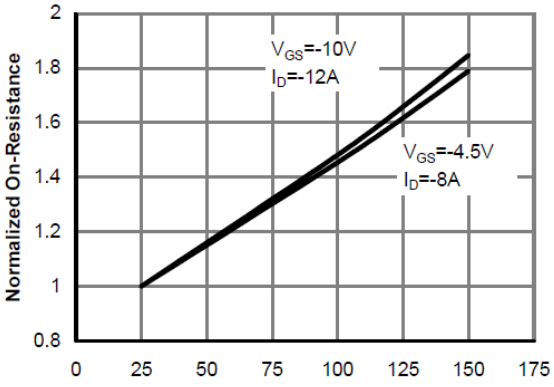


Figure 4: On-Resistance vs. Junction Temperature

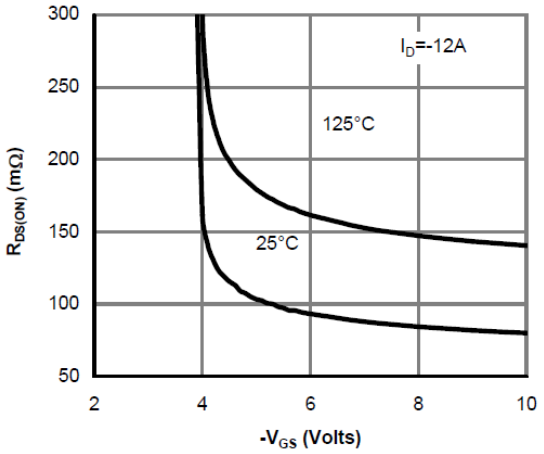
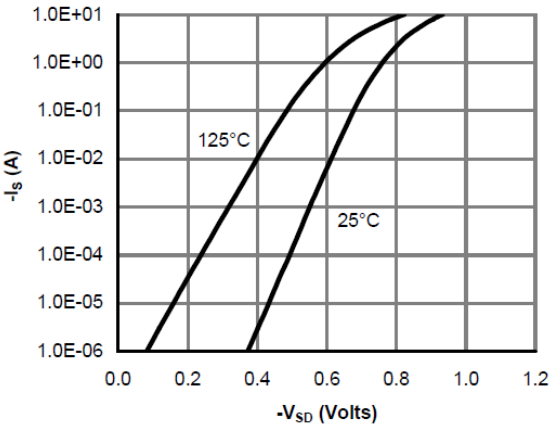


Figure 5: On-Resistance vs. Gate-Source Voltage



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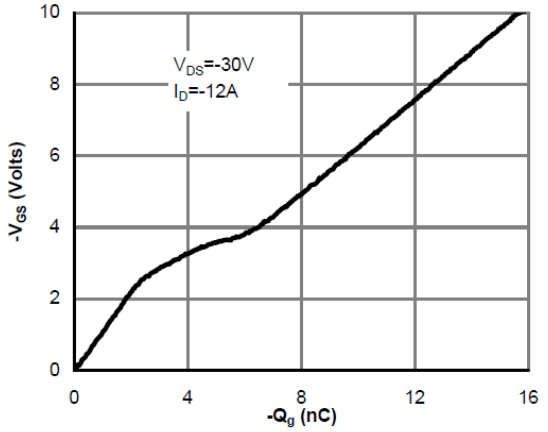

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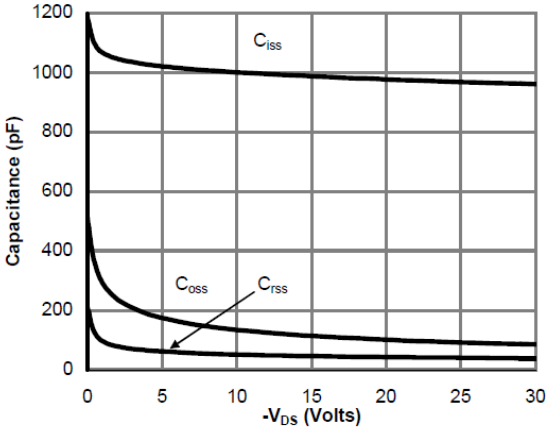

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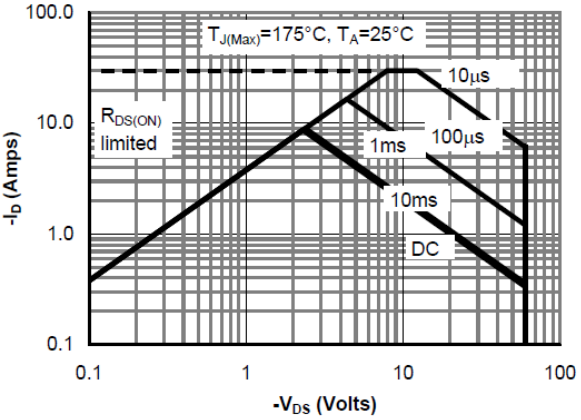

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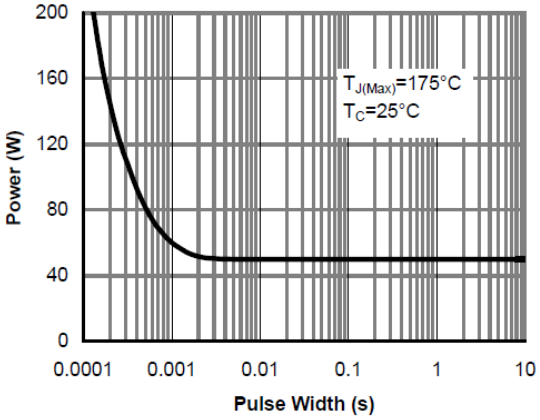

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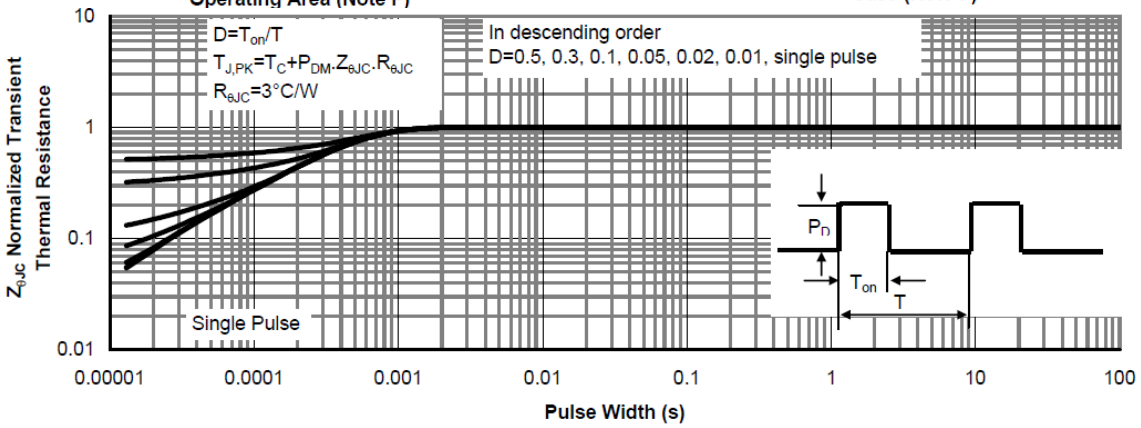
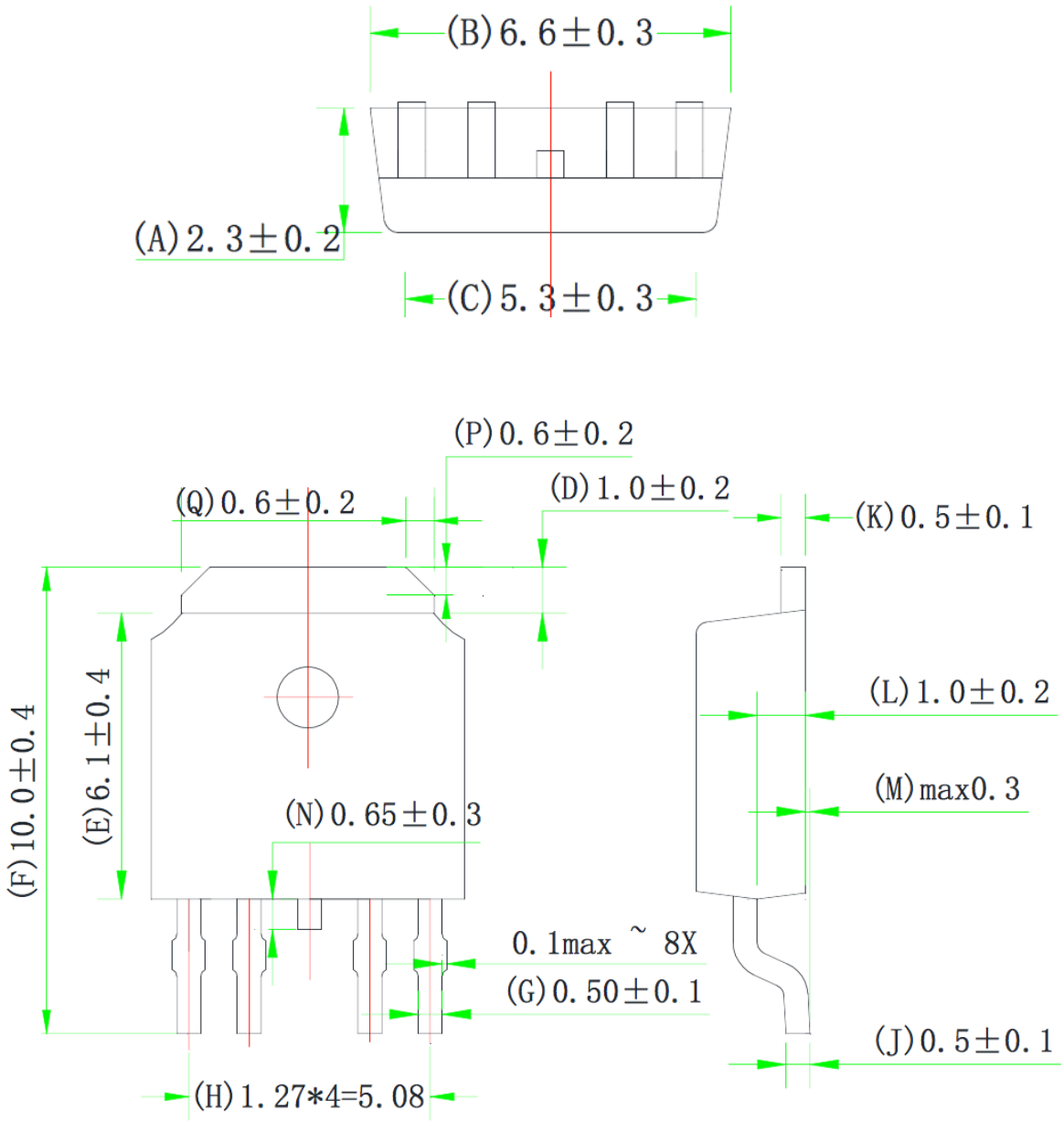


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TO252-4L PACKAGE OUTLINE



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